

**In the Claims**

1 1. (Previously Presented) A phase-locked loop bandwidth calibration circuit, comprising:  
2 a programmable charge pump;  
3 a phase-locked loop filter operatively connected to said programmable charge pump;  
4 an oscillator, operatively connected to said phase-locked loop filter, to generate a  
5 frequency signal based upon a signal received from said phase-locked loop filter; and  
6 a control loop operatively connected to said phase-locked loop filter and said  
7 programmable charge pump;  
8 said control loop including a gain measurement circuit, operatively connected to said  
9 oscillator, to measure a gain of said oscillator;  
10 said control loop controlling said programmable charge pump to adjust its output current  
11 level based on the measured gain of said oscillator;  
12 said gain measurement circuit including,  
13 a voltage difference measurement circuit, operatively connected to said  
14 phase-locked loop filter, to measure a voltage difference corresponding to two  
15 voltages being output from said phase-locked loop filter at different times,  
16 an analog to digital converter, operatively connected to said voltage  
17 difference measurement circuit, to convert the measured voltage difference into a  
18 digital signal, and  
19 a controller to cause said programmable charge pump to adjust its output  
20 current level based upon a received digital signal from said analog to digital  
21 converter.

1 **Claim 2 (Cancelled)**

1 3. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,  
2 wherein said control loop controls said programmable charge pump to adjust its output current  
3 level so that the product of the measured gain and a charge pump current level is kept constant.

1           4. (Previously Presented) The phase-locked loop bandwidth calibration circuit as claimed  
2 in claim 1, further comprising:

3           a voltage reference circuit, operatively connected to said programmable charge pump and  
4 said analog to digital converter, to generate and apply a same reference voltage to said  
5 programmable charge pump and said analog to digital converter based upon changes in a  
6 reference voltage.

1           5. (Previously Presented) The phase-locked loop bandwidth calibration circuit as claimed  
2 in claim 1, further comprising:

3           an integer-N divider operatively connected to an output of said oscillator; and

4           a phase and frequency detector operatively connected between said integer-N divider and  
5 said programmable charge pump.

1           6. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 5,  
2 wherein said control loop controls said programmable charge circuit to adjust its output current  
3 level so that the product of the measured gain and a charge pump current level divided by an  
4 average N value, said N value being provided by said integer-N divider, is kept constant.

1           7. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,  
2 further comprising:

3           an integer-N divider operatively connected to an output of said oscillator;

4           a sigma-delta-modulator operatively connected to said integer-N divider; and

5           a phase and frequency detector operatively connected between said integer-N divider and  
6 said programmable charge pump.

1           8. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 7,  
2 wherein said control loop controls said programmable charge pump to adjust its output current  
3 level so that the product of the measured gain and a charge pump current level divided by an  
4 average N value, said N value being provided by said integer-N divider, is kept constant.

1           9. (Previously Presented) A phase-locked loop bandwidth calibration circuit, comprising:  
2           a programmable charge pump;  
3           a phase-locked loop filter operatively connected to said programmable charge pump;  
4           an oscillator, operatively connected to said phase-locked loop filter, to generate a  
5 frequency signal based upon a signal received from said phase-locked loop filter;  
6           a control loop operatively connected to said phase-locked loop filter and said  
7 programmable charge pump;  
8           said control loop including a gain measurement circuit, operatively connected to said  
9 oscillator, to measure a gain of said oscillator;  
10          said control loop controlling said programmable charge pump to adjust its output current  
11 level based on the measured gain of said oscillator;  
12          a programmable gain amplifier;  
13          a comparator for comparing a voltage of an output from said programmable gain  
14 amplifier with a voltage necessary to produce a predetermined frequency shift in said oscillator  
15 to produce a gain signal; and  
16          a gain controller, in response to said gain signal produced by said comparator, to control  
17 a gain of said programmable gain amplifier.

1           10. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 9,  
2 wherein said gain controller includes a counter and a plurality of resistors, said plurality of  
3 resistors being switchable into or out of a circuit connected between an output of said  
4 programmable gain amplifier and an input of said programmable gain amplifier.

1           11. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 9,  
2 wherein said gain controller controls the gain of said programmable gain amplifier such that a  
3 full scale input to said programmable gain amplifier produces said predetermined frequency shift  
4 in said oscillator.

12. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1, wherein said phase-locked loop filter includes a capacitor; a charging circuit to pre-charge said capacitor to a voltage of said phase-locked loop filter; and a switch to switch said capacitor into the phase-locked loop filter circuit to effect a phase-locked loop bandwidth.

13. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1, wherein said phase-locked loop filter includes a dual path having an integrator path and a lead-lag path.

14. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 13, wherein said programmable charge pump provides a first current output level to said integrator path and a second current output level to said lead-lag path.

**Claims 15-26 (Cancelled)**

27. (Currently Amended) A method of calibrating a phase-locked loop bandwidth, comprising:

- (a) setting a phase-locked loop at a local oscillator offset;
- (b) allowing the phase-locked loop to settle;
- (c) measuring, after allowing the phase-locked loop set to the local oscillator offset to settle, a first voltage of a voltage-controlled oscillator located in the phase-locked loop;
- (d) setting the phase-locked loop to a channel center frequency;
- (e) allowing the phase-locked loop to settle;
- (f) measuring, after allowing the phase-locked loop set to the channel center frequency to settle, a second voltage of the voltage-controlled oscillator;
- (g) determining a difference between the first and second voltage measurements; and
- (h) controlling a programmable charge circuit located in the phase-locked loop to adjust its output current level based on the determined voltage difference.

1           28. (Original) The method as claimed in claim 27, wherein the programmable charge  
2 circuit adjusts its output current level so that the product of a measured gain and a charge pump  
3 current level is kept constant.

1           **Claims 29-39 (Cancelled)**